WHAT IS CLAIMED IS:

1. A processor comprising:

a segment register configured to store a segment selector locating a segment descriptor; and

an execution core coupled to the segment register, wherein the execution core is configured to:

(i) execute a first instruction specifying the segment register, the execution core being selectively responsive to the segment descriptor during execution of the first instruction dependent on which of a plurality of protected operating modes is active in the processor; and

(ii) update the segment register in response to a segment load instruction independent of which of the plurality of protected operating modes is active.

2. The processor as recited in claim 1 wherein, in a first protected operating mode of the plurality of protected operating modes, a virtual address has greater than 32 bits.

3. The processor as recited in claim 2 wherein the execution core is not responsive to the segment descriptor if the first protected operating mode is active.

4. The processor as recited in claim 3 wherein the execution core is responsive to the segment descriptor if a different one of the plurality of protected operating modes is active.

5. The processor as recited in claim 1 further comprising a second segment register configured to store a second segment selector locating a second segment descriptor, wherein the execution core is coupled to the second segment register and is configured to execute a second instruction specifying the second segment register, and wherein the execution core is responsive to the second segment descriptor during execution of the second instruction independent of which of the plurality of protected operating modes is active.

6. The processor as recited in claim 1 wherein, prior to updating the segment register in response to the segment load instruction, the execution core is configured to check the segment descriptor for one or more exception conditions, and wherein the execution core is configured to signal an exception instead of updating the segment register if at least one of the one or more exception conditions is detected.

7. An apparatus comprising:

a storage location corresponding to a segment register, the storage location storing a segment selector locating a segment descriptor; and

a processor configured to:

(i) process a first instruction specifying the segment register, including selectively responding to the segment descriptor during processing of the first instruction dependent on which of a plurality of protected operating modes is active; and

(ii) update the storage location in response to a segment load instruction independent of which of the plurality of protected operating modes is active.

8. The apparatus as recited in claim 7 wherein, in a first protected operating mode of the plurality of protected operating modes, a virtual address has greater than 32 bits.

9. The apparatus as recited in claim 8 wherein the processing of the first instruction does not include responding to the segment descriptor if the first protected operating mode is active.

10. The apparatus as recited in claim 9 wherein the processing of the first instruction does include responding to the segment descriptor if a different one of the plurality of protected operating modes is active.

11. The apparatus as recited in claim 7 further comprising a second storage location corresponding to a second segment register, the second storage location storing a second segment selector locating a second segment descriptor, wherein the processor is configured to process a second instruction specifying the second segment register, and wherein the processing is responsive to the second segment descriptor independent of which of the plurality of protected operating modes is active.

12. The apparatus as recited in claim 7 wherein, prior to updating the storage location in response to the segment load instruction, the processor is configured to check the segment descriptor for one or more exception conditions, and wherein the processor is configured to signal an exception instead of updating the storage location if at least one of the one or more exception conditions is detected.

13. A method comprising:

executing a first instruction specifying a segment register, the executing including selectively responding to a segment descriptor indicated by a segment

selector in the segment register, the selectively responding dependent on which of a plurality of protected operating modes is active; and

updating the segment register in response to a segment load instruction independent of which of the plurality of protected operating modes is active.

14. The method as recited in claim 13 wherein, in a first protected operating mode of the plurality of protected operating modes, a virtual address has greater than 32 bits.

15. The method as recited in claim 14 wherein the selectively responding includes not responding to the segment descriptor if the first protected operating mode is active.

16. The method as recited in claim 15 wherein the selectively responding includes responding to the segment descriptor if a different one of the plurality of protected operating modes is active.

17. The method as recited in claim 13 further comprising executing a second instruction specifying a second segment register configured to store a second segment selector locating a second segment descriptor, wherein the executing is responsive to the second segment descriptor independent of which of the plurality of protected operating modes is active.

18. The method as recited in claim 13 further comprising:

prior to the updating, checking the segment descriptor for one or more exception conditions; and

signalling an exception instead of the updating if at least one of the one or more

exception conditions is detected.

19. A method comprising:

loading one or more segment descriptors into segment registers, the loading performed in a first protected operating mode in which at least one of the one or more segment descriptors is not used even if an instruction specifying the corresponding segment register is executed; and

branching to a code segment which establishes a second protected operating mode in which the one or more segment descriptors are used.

20. The method as recited in claim 19 wherein the loading comprises:

checking the segment descriptors for one or more exception conditions; and

exiting to an exception handler instead of loading one of the segment descriptors responsive to the checking detecting at least one of the one or more exception conditions in the one of the segment descriptors.